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ABSTRACT

A ferroelectric field-effect transistor (FeFET) with scaled dimensions (170 nm and 24 nm of gate width and length, respectively) and a 10 nm thick Si doped HfO_2 ferroelectric in the gate oxide stack are characterized at cryogenic temperatures down to 6.9 K. We observe that a decrease in temperature leads to an increase in the memory window at the expense of an increased program/erase voltage. This is consistent with the increase in the ferroelectric coercive field due to the suppression of thermally activated domain wall creep motion at cryogenic temperatures. However, the observed insensitivity of the location of the memory window with respect to temperature cannot be explained by the current understanding of the device physics of FeFETs. Such temperature dependent studies of scaled FeFETs can lead to useful insights into their underlying device physics, while providing an assessment of the potential of this emerging technology for cryogenic memory applications.

The discovery of ferroelectricity in doped/alloyed hafnium oxide[1] opens up a pathway for ferroelectric field-effect transistors (FeFETs), which were first demonstrated in 1974,[2] to be integrated with the readily available complementary metal-oxide-semiconductor (CMOS) platform thanks to the scalability and CMOS compatibility of hafnium oxide. FeFETs are emerging as an important memory and computation element for embedded non-volatile memory, near-memory computation, and bio-mimetic computing applications owing to their nanosecond program/erase time, low voltages, and dense analog states.[3–8]

Ferroelectricity, being a phase transition, exhibits a strong temperature dependence. Temperature dependent studies of ferroelectric materials provide useful insights into the intrinsic and extrinsic factors determining their functional properties and, hence, are of fundamental importance in understanding these materials. While the properties of archetypal perovskite based ferroelectrics have been studied in great detail over the last seven decades all the way from above 1400 K down to the mK range,[9–12] there exist only a few similar studies on the fluorite type simple, binary oxide ferroelectrics (i.e., HfO_2 based ones) limited to a temperature range of 77 K and 1200 K.[13–17] Recently, antiferroelectricity—a phenomenon closely related to ferroelectricity—in a similar material system (ZrO_2) was studied down to 50 mK.[18] Even more so, the properties of ferroelectric field-effect-transistors, wherein the characteristic temperature dependence of the ferroelectric oxide and the semiconductor channel are completely disparate, can evolve in a complicated way with temperature, which can allow for an interesting pathway of understanding the device physics of this emerging technology. To date, FeFETs have only been characterized at elevated temperatures to assess their retention and endurance properties,[3,4,19] leaving the cryogenic regime an uncharted territory.

From a technology perspective, cryogenic memory systems operating in all ranges between room temperature and ~mK are of significant interest. For aerospace and space electronics, the cryogenic computing and memory elements are critically important. In the context of cloud based, high performance computing, especially for machine learning and data analytics applications, performance is the key driver; 77 K memory technologies are being investigated to deliver massive leaps in iso-reliability performance.[20] Superconducting single flux quantum (SFQ) digital processors based on Josephson junctions

(JJ) at 4 K require a compatible memory technology operating at the same temperature.[20] In a recent breakthrough, solid state quantum computers and quantum bits (qubits) are placed inside a dilution-refrigerator at a few tens of mK connected to the control processor at room temperature through control cables. The existing superconducting memory technologies (such as the JJ based memories[21] and hybrid JJ-CMOS memories[22]) operating at mK cannot be used as the sole memory technology due to their limited memory density and energy efficiency. Considerations with regard to refrigerator cooling power, thermal leakage, space constraints, and so on essentially require memory architectures with a hierarchical structure where the amortized, classical memory systems are arranged at different temperature stages.[23,24] Altogether, expanding the application space of cryogenic computing and memory technologies can create opportunities for the emerging non-volatile memories such as FeFETs.

In this Letter, we investigate the cryogenic characteristics of an n-type FeFET fabricated on a GLOBALFOUNDRIES 22 nm planar fully depleted silicon-on-insulator (FDSOI) platform.[4] A 10 nm silicon doped hafnium oxide (Si : HfO_2) ferroelectric layer is included in the FeFET gate oxide stack. The physical width (W) and the gate length (L) of the FeFET are 170 nm and 24 nm, respectively. The device was characterized in a Lake Shore TTP6 cryogenic probe station using an Agilent 4156C Semiconductor Parameter Analyzer. Figures 1(a)–1(j) show the d.c. drain current I_D vs gate voltage V_{GS} characteristics of the FeFET in the linear (drain voltage $V_{DS} = 50$ mV) and saturation ($V_{DS} = 1$ V) regions at $T = 300$ K, 200 K, 80 K, 20 K, and 6.9 K, respectively. The I_D -V_{GS} curves of $T = 300$ K are plotted in the background for comparison in Figs. 1(c)–1(j). Counterclockwise hystereses are observed in the I_D - V_{GS} curves, which correspond to the dominated ferroelectric switching effect. However, clockwise hystereses are also detected for V_{GS} values beyond ~1.7 V, which is typically attributed to charge trapping.[25] The subthreshold swing (S) in the forward sweep direction (from −3 V to 3 V), determined by the linear fitting of $\ln(I_D)$ where I_D is between 10^{-4} μA and 10^{-3} μA for $V_{DS} = 50$ mV and I_D is between $5 \cdot 10^{-4}$ μA and 10^{-2} μA for $V_{DS} = 1$ V, is plotted as a function of temperature for $V_{DS} = 50$ mV and 1 V in Figs. 2(a) and 2(b), respectively. In these figures, the ideal temperature scaling law of S: $S \propto k_B T \ln(10)/q$ with k_B and q being the Boltzmann constant and elementary charge, respectively, is also plotted. We observe in Figs. 2(a) and 2(b) that above ~220 K, forward S deviates from the scaling law, which indicates a strong influence of thermally activated interface traps in the subthreshold region of the forward sweep characteristics.[26] On the other hand, steep transitions are observed in the backward sweep direction (from 3 V to −3 V) of the I_D - V_{GS} characteristics the slope of which is fairly independent of temperature. Generally, such characteristics are solely attributed to ferroelectric domain switching and charge de-trapping.[27] These two mechanisms lead to a minimum subthreshold swing S below 10 mV/dec even at $T = 300$ K, overshadowing the effect of the temperature scaling law of S. Figures 2(c) and 2(d) show the evolution of I_D of the upper branch of the hysteresis loop at $V_{GS} = 3$ V and 0 V with $V_{DS} = 50$ mV and 1 V, respectively. As the temperature decreases, I_D at $V_{GS} = 3$ V in both linear and saturation regions increases initially and then flattens out. This phenomenon is possibly due to mobility degradation due to increased phonon scattering at higher temperatures. On the other hand, I_D at $V_{GS} = 0$ V shows a small bump around $T = 250$ K and remains roughly constant below 100 K. Note that I_D at $V_{GS} = 0$ V and

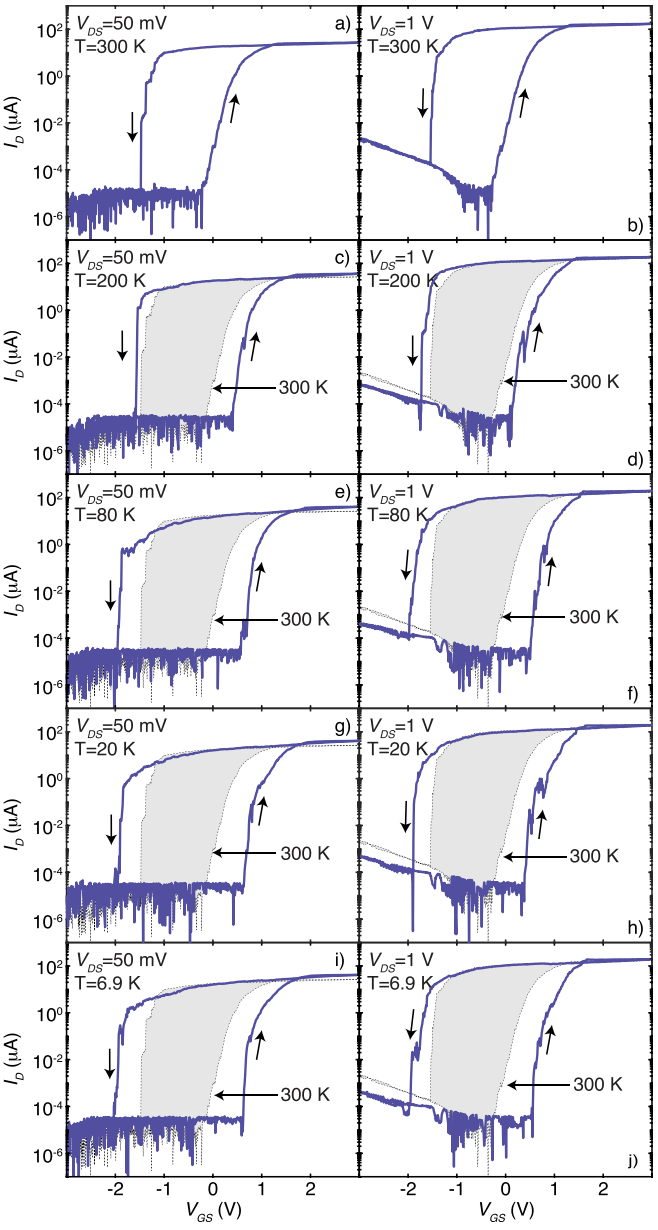

FIG. 1. (a)–(j) d.c. I_D - V_{GS} transfer characteristics of a FeFET with $W = 170$ nm and $L = 24$ nm at $V_{DS} = 50$ mV and 1 V for $T = 300$ K, 200 K, 80 K, 20 K, and 6.9 K, respectively. I_D - V_{GS} curves of $T = 300$ K are plotted as the background for comparison in (c)–(j).

I_D at $V_{GS} = 3$ V show different trends for T above 150 K; however, the exact reason for this is not known to the authors.

Next, we study how the memory window evolves as the temperature is changed. The memory window is defined as the difference of the threshold voltages in the forward and the reverse sweep directions, V_{T1} and V_{T2}, respectively—i.e., $MW = V_{T1} - V_{T2}$. The threshold voltages are defined as the gate voltage at which I_D per unit width reaches 1 μA/μm (i.e., $I_D = 0.17$ μA). Figures 3(a) and 3(b) plot V_{T1}

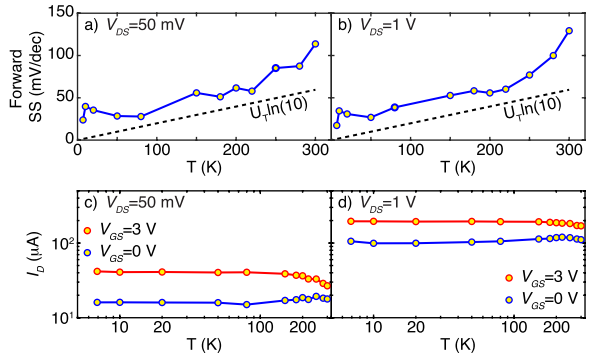

FIG. 2. (a) and (b) Subthreshold swing of the FeFET in the forward sweep direction (from −3 V to 3 V) as a function of temperature for $V_{DS} = 50$ mV and 1 V, respectively. (c) and (d) FeFET on-current at $V_{GS} = 3$ V and 0 V as a function of temperature for $V_{DS} = 50$ mV and 1 V, respectively.

and $|V_{T2}|$ as functions of temperature at $V_{DS} = 50$ mV and 1 V, respectively. Figures 3(c) and 3(d) plot the temperature evolution of the width of the memory window MW at $V_{DS} = 50$ mV and 1 V, respectively. Figures 3(e) and 3(f) show the evolution of the center of the memory window, which is defined as $(V_{T1} + V_{T2})/2$, at $V_{DS} = 50$ mV and 1 V, respectively, with temperature. We observe in these figures that as temperature decreases from 300 K to 6.9 K, both V_{T1} and $|V_{T2}|$ increase by ∼0.5 V, resulting in an ∼1 V increase in the memory window. On the other hand, the center of the memory window stays rather independent of temperature. The MW vs T curves for $V_{DS} = 50$ mV and $V_{DS} = 1$ V shown in Figs. 3(c) and 3(d) can be fitted to the following linear equation by averaging the coefficients obtained from different V_{DS},

$$MW[\![V]\!] = -4.42 \times 10^{-3}\left[\!\left[\frac{V}{K}\right]\!\right] T[\![K]\!] + 3.04\,[\![V]\!]. \tag{1}$$

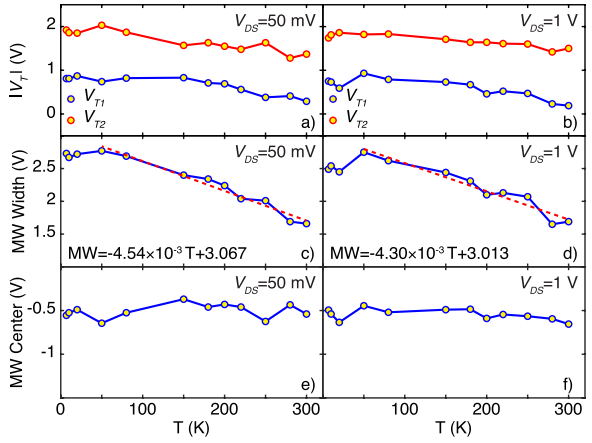

FIG. 3. (a) and (b) Threshold voltages V_{T1} and V_{T2} of the FeFET vs temperature at $V_{DS} = 50$ mV and 1 V, respectively. Threshold voltages are defined as the gate voltage where the drain current reaches 0.17 μA. (c) and (d) Memory window (MW) width of the FeFET vs temperature at $V_{DS} = 50$ mV and 1 V, respectively. For temperatures between 50 K and 300 K, the memory window size can be fitted by Vopsaroiu's model.[30] (e) and (f) Memory window (MW) center of the FeFET vs temperature at $V_{DS} = 50$ mV and 1 V, respectively.

Note that the memory window of a FeFET can be estimated as[28]

$$MW = 2t_{FE}E_C \approx V_{T1} - V_{T2}, \tag{2}$$

where t_{FE} and E_C are the thickness and the coercive field of the ferroelectric layer, respectively. To understand the temperature dependence of the constituent ferroelectric in the FeFET, we note that at $T = 0$ K, ferroelectric switching has a well-defined coercive field $E_{C,i}(T = 0)$, which is described within the Landau theory. In this case, the domain wall velocity is zero below $E_{C,i}(0)$ and above $E_{C,i}(0)$, and the domain walls undergo a pinning–depinning transition and have a finite velocity.[11] At a finite temperature T, the pinning–depinning transition is smoothed out by the thermal energy. As a result, in the low electric field $[E \ll E_{C,i}(T)]$ creep regime, the domain walls propagate at a non-zero velocity.[11] Altogether, due to the combined effects of the thermal fluctuations[29] and the applied electric field, the thermally activated domain wall creep motion gets increasingly suppressed, and the number of nucleation centers is reduced at low electric fields with the decrease in temperature. Therefore, the electric field at which ferroelectric polarization switching occurs—i.e., the observed coercive field E_C—gets closer to the intrinsic coercive field at cryogenic temperatures, resulting in an increase in MW. According to Vopsaroiu's model,[30] which has been previously utilized to analyze the temperature dependence in Si doped HfO_2,[13] the coercive field and the temperature are related by the following relation:

$$E_C \cong \frac{W_B}{P_s} - \frac{k_B T}{V^* P_s}\ln\left(\frac{\nu_0 \tau}{\ln(2)}\right), \tag{3}$$

where W_B is the energy barrier per unit volume, P_s is the spontaneous polarization, ν_0 is the soft mode attempt frequency, V^* is the critical nucleation activation volume, and τ is the time scale of the measurement. Even though the energy barrier per unit volume W_B and critical nucleation activation volume V^* are known to be temperature dependent, in Vopsaroiu's model,[30] they are constant material parameters determined in the vicinity of zero Kelvin. In our FeFETs, $t_{FE} = 10$ nm and $\tau \approx 5$ s. Combining Eqs. (1)–(3) and using first principles calculation based values, $P_s = 0.41$ C/m^2 and $\nu_0 = 1.16 \times 10^{13}$ Hz,[31] we obtain a critical nucleation activation volume V^* of 4.88 nm^3 and an energy barrier ($W_B \times V^*$) of 1.9 eV for the Si doped HfO_2 ferroelectric layer in the FeFET by fitting the memory window size from 50 K to 300 K. These values are close to the values estimated for Si doped HfO_2 in capacitor structures in Ref. 13 ($V^* = 3.47$ nm^3 and $W_B \times V^* = 1.38$ eV).

To study the effects of the voltage sweep range on the memory window as the temperature is changed, the following measurement protocol is executed. The drain voltage V_{DS} was held at 50 mV, and the gate voltage V_{GS} was swept from −3 V up to V_{max} and then swept back to −3 V. V_{max} was varied from 0 V to 3 V. Figures 4(a)–4(j) show d.c. $I_D - V_{GS}$ characteristics for different values of V_{max} at $T = 11$ K and 300 K. Again, we define the memory window as the difference in the threshold voltage at which I_D per unit width reaches 1 μA/μm, below which we consider as no memory window. We observe that at $T = 11$ K, no hysteresis opens up for V_{max} below 1 V. As V_{max} increases up to 2 V, a clockwise hysteresis opens up, which is attributed to charge trapping.[25] For $V_{max} = 2.2$ V, the polarization is partially switched, and the FeFET shows a counterclockwise hysteresis with a reduced memory window. An increase in V_{max} above 2.2 V leads to a larger memory window. In contrast, at $T = 300$ K, clockwise

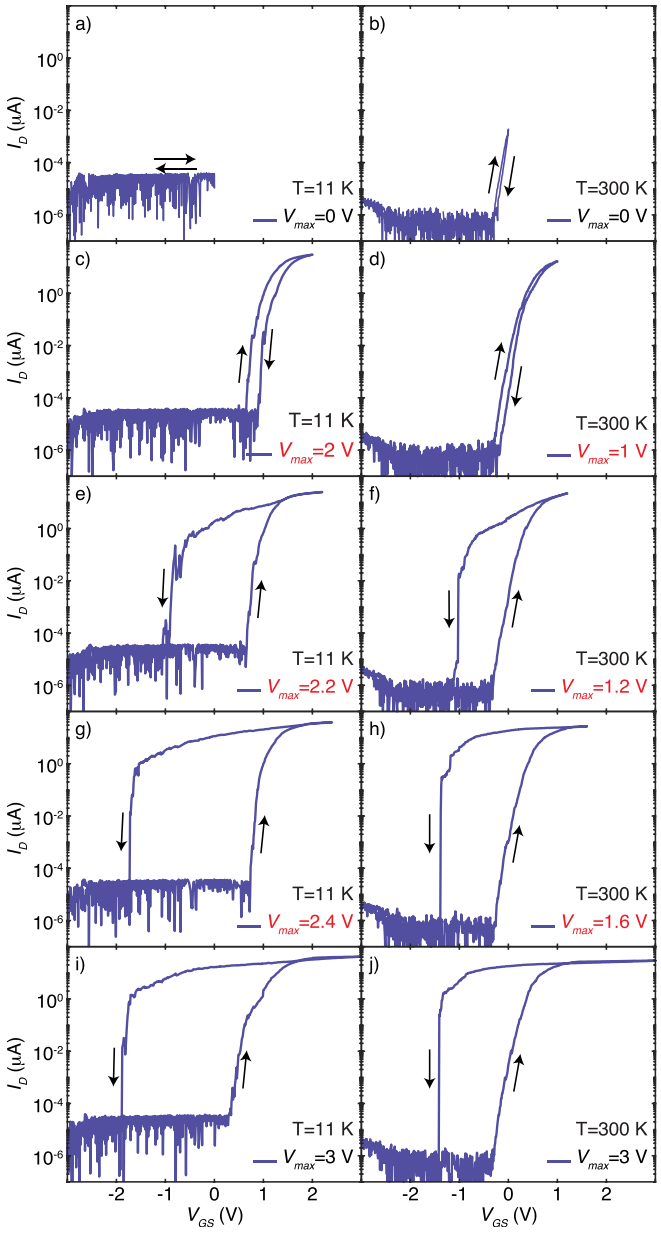

FIG. 4. (a)–(j) d.c. I_D - V_{GS} transfer characteristics of the FeFET for different voltage sweep ranges sweeping from −3 V to V_{max} at $T = 11$ K and 300 K. For $T = 300$ K, the measurement was performed in a Cascade 12 K semiautomatic probe station, and therefore, the current noise floor is lower. At cryogenic temperature, a higher gate voltage is required to initiate the ferroelectric switching.

hysteresis appears for V_{max} less than 1 V. At $V_{max} \geq 1.2$ V, the FeFET exhibits a counterclockwise hysteresis loop. Notice that the I_D - V_{GS} curves for which $V_{max} > 2.4$ V [Fig. 4(i) and supplementary Figs. S2 and S3(e)] show a sudden decrease in V_{T1} and V_{T2} and smoother slopes in the subthreshold region. This phenomenon, only prominent at cryogenic temperature, is not understood at this moment and requires further studies. Figure 5 summarizes how the voltage range

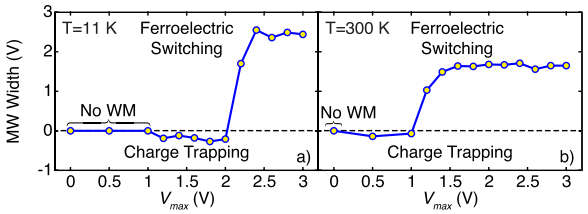

FIG. 5. (a) and (b) Memory window (MW) width as a function of V_{max} at $T = 11$ K and 300 K, respectively. The negative memory window is due to charge trapping, and the positive memory window is because of ferroelectric switching. At cryogenic temperature, a higher voltage is required to switch the FeFET due to the suppression of thermally activated domain wall creep motion and the reduced number of activated domain nucleation regions.

for charge trapping and ferroelectric switching evolves as the temperature is changed between 11 K and 300 K—by plotting the memory window as a function of V_{max} at these temperatures.

It is rather a curious observation that the observed temperature dependence of the location of the memory window [Figs. 3(c) and 3(d)] cannot be explained solely by the expected temperature evolution of E_C and the intrinsic carrier density in the semiconductor channel. In conventional n-type CMOS transistors, a decrease in temperature decreases the intrinsic carrier density n_i, which makes the threshold voltage more positive. For example, in 28 nm FDSOI transistors, the difference between the threshold voltages at 4 K and 300 K is of the order of 200 mV.[32] As such, the temperature dependence of the semiconductor channel in an FeFET is expected to contribute similar positive shifts to the forward and reverse sweep threshold voltages (V_{T1} and V_{T2}, respectively).

On the other hand, the increase in E_C with the lowering of temperature contributes a positive and a negative shift to V_{T1} and V_{T2}, respectively. As such, the change in V_{T1} is expected to be larger than that in V_{T2}, resulting in a positive shift in the center of the memory window with the decrease in the temperature—as opposed to what is observed in Figs. 3(e) and 3(f). This suggests that defects/traps, the pyroelectric effect of doped hafnium oxide,[33] and yet-to-be-understood extrinsic factors affect the forward and reverse sweep threshold voltages differently, leading to the relative temperature insensitivity of the memory window location.

In summary, the cryogenic characterization of scaled ferroelectric field-effect-transistors (FeFETs) reveals that a decrease in the temperature leads to an increase in the memory window at the expense of an increased program/erase voltage. This is consistent with the increase in the ferroelectric coercive field with the lowering of temperature. On the other hand, the current understanding of FeFETs cannot clearly explain the temperature evolution of the location of the memory window. Given that the studied FeFET is extremely scaled in the lateral directions (of the order of 100 nm) with only a few ferroelectric grains, the switching dynamics is not well described within the traditional ferroelectric models.[34–37] Hence, temperature dependent studies of ferroelectric field-effect transistors can provide insights into their device physics and the underlying physics of ferroelectrics at uncharted, mesoscopic length scales.

See the supplementary material for additional d.c. I_D - V_{GS} transfer characteristics of FeFETs and V_{T1} and V_{T2} as a function of V_{max}.

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